IN THE CLAIMS

1. (currently amended) An apparatus comprising:

a plurality of storage locations for storing packets received from a network;

a system for dynamically ~~calculating~~ updating a probability distribution associated with packet network delays ~~for plural packets~~; and

a ~~CPU~~ processor for calculating, based upon said dynamically ~~calculated~~ updated probability distribution, a delay associated with each storage location, and for causing a packet in each storage location to be transmitted out of the storage location after being stored in the storage location an amount of time equal to the associated delay. ~~associated with the storage location.~~

2. (currently amended) The apparatus of claim 1 wherein the ~~CPU~~ processor, in calculating ~~said~~ the associated delay ~~for a packet~~, calculates a difference between ~~the~~ an optimal delay permissible to guarantee a predetermined probability of packet loss[[,]] and an actual delay experienced by the packet for which the calculation is being done.

3. (currently amended) The apparatus of claim 2 wherein the probability distribution is updated every Nth packet received~~, where N is a positive integer~~.

4. (currently amended) The apparatus of claim 3 wherein N is 1.

5. (currently amended) An apparatus comprising:

plural buffers;

a Central Processing Unit (CPU) for causing packets arriving from a network at said apparatus to each be stored in a separate one of the buffers, the CPU also being arranged to calculate, upon receipt of every Nth packet of data, an ~~dynamically adapted~~ optimal delay beyond which a packet will be ~~lost~~ discarded, the optimal delay being calculated using a probability distribution that is updated upon the receipt of each packet; and

a timer for causing each packet to incur an added delay ~~at the gateway~~ of at least the difference between the calculated optimal delay and ~~the~~ an actual network delay experienced by said each packet.

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6. (currently amended) The apparatus of claim 5 wherein N is greater than or equal to 1.

7. (canceled)

8. (currently amended) The apparatus of claim 5 further comprising a network interface card coupled to the CPU for receiving signals from the data network.

9. (currently amended) The apparatus of claim 5 wherein the CPU is a Digital Signal Processing (DSP) chip that performs DSP, CPU control and input/output ~~and control~~ functions.

10. (currently amended) The apparatus of claim 8 wherein said network interface card implements the G.723 or G.729 standard.

11. (currently amended) A method of processing packets comprising:

[[a.]] receiving a packet;

updating a probability distribution;

updating an optimal delay that is based at least in part on the updated probability distribution;

[[b.]] reading information in the packet and ascertaining therefrom a delay incurred by the packet in traversing the network;

[[c.]] comparing the delay ascertained to ~~a dynamically adapted~~ the optimal delay; and

[[d.]] delaying use of the packet to reconstruct a signal by a calculated amount of time sufficient to make the calculated amount plus the ascertained delay substantially equal to the optimal delay.

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12. (currently amended) The method of claim 11 further comprising setting said optimal delay ~~at an amount equal~~ to a minimum delay ~~required~~ to cause a ~~specified~~ predetermined probability of packet loss.

13. (currently amended) The method of claim 11 wherein said required minimum delay is recalculated every Nth packet~~, where N is a positive integer~~.

14. (currently amended) The method of claim 13 further comprising comparing said ~~required~~ minimum delay to a predetermined value each time said ~~required~~ minimum delay is recalculated, and, if said recalculated ~~required~~ minimum delay exceeds said predetermined value, assigning

said required minimum delay to be said predetermined value ~~instead of said recalculated required minimum delay~~.

15. (currently amended) A gateway comprising:

a buffer for storing said received packets;

a CPU for updating a probability distribution upon the receipt of each packet and for calculating a delay to which each of a plurality of received packets should be subjected before being read out of the buffer;

~~a buffer for storing said received packets;~~

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a timer for subjecting each packet to a calculated delay that equals an ~~dynamically adapted~~ optimal delay, the optimal delay being dynamically updated based at least in part on the updated probability distribution, minus a network delay experienced by the packet, unless such calculated delay exceeds a predetermined maximum, in which case the predetermined maximum is utilized as the calculated delay.

16. (currently amended) A method of measuring varying delays among a plurality of packets, ~~the method~~ comprising:

receiving a first packet at a receiving gateway;

~~fixing~~ maintaining constant any synchronization error between a transmitting gateway and the receiving gateway ~~to a~~ by inserting ~~reasonable value of~~ a delay said packet is estimated to have experienced in traversing a network; and

setting a clock at said receiving gateway to a value equal to a time stamp contained within said first packet plus said ~~reasonable value~~ estimated delay.

17. (currently amended) The method of claim 16 further comprising receiving packets in addition to said first packet, reading a time stamp from each of said additional packets, calculating a network delay for each of said additional packets based upon said clock at said receiving gateway and said timestamp from each of said additional packets.

18. (currently amended) The method of claim 16 further comprising updating a probability distribution function indicative of network delays after receipt of every Nth packet~~, where N is a positive integer~~.

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19. (canceled)

20. (original) The method of claim 18 wherein said updating further comprises recalculating a buffer latency.

21. (currently amended) The method of claim 20 wherein said buffer latency is assigned a value different from the recalculated buffer latency ~~if and~~ only if said recalculated buffer latency exceeds a predetermined value.

22. (original) Apparatus comprising:

a signal processor for calculating a delay experienced by each of a plurality of packets through a data network; and

a buffer system for delaying further conveyance of each of said packets by an amount of time dependant upon (1) a probability distribution updated in response to receipt and processing of selected ones of each of said packets, and (2) said calculated delay.

23. (original) Apparatus of claim 22 wherein said buffer system is arranged to delay further conveyance by an amount also dependant upon a prestored maximum.

24. (original) Apparatus of claim 23 wherein said signal processor is programmed to use a recursive algorithm.

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25. (original) Apparatus of claim 23 further comprising an interrupt generator for generating an interrupt when said amount of time for said each packet expires.

26. (original) Apparatus of claim 23 further comprising a poller for sequentially polling each of a plurality of storage locations within said buffer system to determine if a packet within said storage location is to be further conveyed.

27. (withdrawn) Timing apparatus comprising:

a processor for reading a time stamp in a received data packet, and for setting a clock a specified amount ahead of said time stamp; and

a receiver for receiving subsequent data packets and measuring delay by comparing a time stamp in each of said subsequent packets to said clock.

28. (withdrawn) Timing apparatus of claim 25 wherein said specified amount is programmed to be a delay indicative of a delay experienced by a packet through a data network.

29. (withdrawn) Timing apparatus of claim 27 further comprising a signal processor for converting data within said received packet and within said subsequent packets to an audio signal.